

<b>Form PTO-1449</b>  <b>LIST OF PRIOR ART CITED BY APPLICANT</b> <i>(Use several sheets if necessary)</i>	ATTORNEY DOCKET NO. <b>YOR920030387US1</b>	SERIAL NO. <b>Not Assigned</b>  <i>10/696, 139</i>
	APPLICANT <b>Rhee et al.</b>	
	FILING DATE <b>October 29, 2003</b>	GROUP ART UNIT <b>Not Assigned</b> <i>2816</i>

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.	PUBLICATION DATE	INVENTOR NAME	CLASS/ SUBCLASS	FILING DATE

## FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.	PUBLICATION DATE	COUNTRY	CLASS/ SUBCLASS	TRANSLATION YES NO	

## OTHER PRIOR ART (including author, title, date, pertinent page, etc.)

<i>un</i>	AA	Sidiropoulos et al., "A Semidigital Dual Delay-Locked Loop", IEEE Journal of Solid-State Circuits, Vol. 32, No. 11, November 1997, pp. 1683-1692.

## RELATED PATENT APPLICATIONS

EXAMINER INITIAL	APPLICATION NO/ ATTY. DOCKET NO.	APPLICANT	TITLE	FILING DATE

DATE CONSIDERED <i>Nov 2, 2004</i>	EXAMINER <i>[Signature]</i>
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